

# EPIC

Enabling Practical Wireless  
Tb/s Communications  
with Next Generation  
Channel Coding

Project reference: **760150**  
Project website: [www.epic-h2020.eu](http://www.epic-h2020.eu)  
Project start: **1<sup>st</sup> September, 2017**  
Duration: **3 years**  
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EC contribution: **EUR 2,966,268.75**



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EPIC 

The EPIC logo graphic consists of three blue chevrons pointing to the right, positioned to the right of the word 'EPIC'.





## Mission of EPIC:

EPIC aims to develop a new generation of Forward-Error-Correction (FEC) codes in a manner that will serve as a fundamental enabler of practicable beyond-5G (B5G) wireless Tb/s solutions and also to develop and utilize a disruptive FEC design allowing to advance state-of-the-art FEC schemes and to obtain the principal channel codes for beyond-5G use-cases. The design framework developed within the project will offer new ways to conduct research and development and has the potential to affect the development of all future B5G communication systems. EPIC will put great emphasis on evaluating the commercial viability of the project outcomes targeting beyond-5G systems.

## Motivation:

The key tenet of EPIC is that a disruptive wireless link technology is fundamental for the birth of each new telecommunication generation. Routine progress in silicon technology in the next decade will not be sufficient to allow FEC implementations to break the Tb/s barrier. Tb/s FEC will require not only help from silicon technology but also major innovations in FEC algorithm design and implementation domains. FEC is a foundational component of any wireless link technology, constituting the most complex and computationally intense component in the baseband chain. The EPIC concept rests on the premise that the leap to Tb/s data rates, and the associated system requirements, call for a paradigm shift in the conventional FEC design and development approach. This is necessary in order to align the FEC design and implementation problem with the novel constraints arising from wireless Tb/s use-cases as well as the emergence of a new design landscape in which energy and power density are becoming the most challenging implementation parameters as silicon technology moves to ever smaller linewidths. Technology evolution observations, from data traffic trends to network infrastructure models, put practical wireless Tb/s technology as the next major milestone, arguably carrying the potential for completely novel telecommunication technology generations unprecedented even in today's 5G vision.

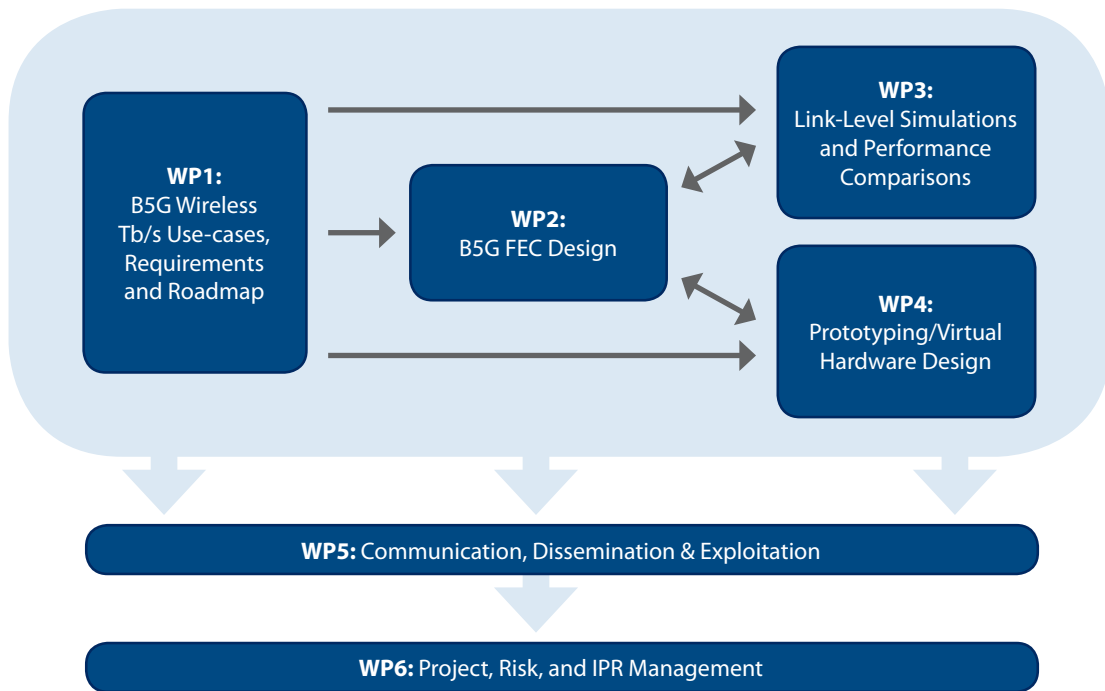
## Concept:

EPIC proposes to develop an implementation-ready FEC technology that meets the cost and performance requirements of a variety of potential wireless Tb/s use-cases. EPIC methodology differentiates itself by combining algorithm design and implementation studies into a whole so that optimization studies can be carried out jointly over a larger domain. Top-performing solutions developed within EPIC will be **validated by virtual silicon tape-out**, thus providing first-in-class FEC blocks of wireless Tb/s technology. Furthermore, EPIC will make major contributions to the scientific community in the fields of **Turbo, LDPC, and Polar code design and implementation**. Thanks to EPIC's comprehensive dissemination plan, the project will engage in cross-project activities to maximize the impact of the work, ensure adoption in related work, and **reaffirm Europe's central role in Information Theory and Digital Signal Processing research**. Industrial partners in EPIC will ensure early identification of commercialization potential and uptake in standardization bodies.

## Objectives:

The EPIC consortium, which includes the lead inventors and institutes in the FEC domain, dynamic SMEs, and impactful industry partners, is dedicated to successfully reach the following objectives:

- **Objective 1:** EPIC will design and implement next generation Forward-Error-Correction for wireless Tb/s technology and beyond-5G systems.
- **Objective 2:** EPIC will advance state-of-the-art codes and develop the principal channel coding technology for wireless Tb/s technology.
- **Objective 3:** EPIC will devise a disruptive FEC design framework to unify algorithmic and implementation domains.
- **Objective 4:** EPIC will validate and demonstrate the developed FEC technology in virtual silicon tape-out and provide first-in-class wireless Tb/s FEC chipset architecture block.
- **Objective 5:** EPIC puts the scientific excellence and contributions to wireless industry in the domain of B5G standardization and technology development at the centre of the project execution.



## Technical Approach:

The EPIC project is planned to run for 36 months and is subdivided into six work packages (WP). Between these WPs there are significant dependencies and expected synergies, which are described shortly in the following:

### WP1: B5G Wireless Tb/s Use-cases, Requirements and Roadmap

This WP will develop the methodologies for using the toolbox developed in WP2. This includes the definition of specific aids and methods adequate for the use-cases of the project as well as GUI (Graphical User Interface) developments to support them.

### WP2: B5G FEC Design

The investigation of interrelations between code structure, encoding and decoding algorithms, communications performance, flexibility and efficient hardware architectures and their implementations in state-of-the-art technologies is the main task of this WP.

Furthermore new encoding/decoding algorithms are developed along with novel B5G channel codes. WP2 also provides hardware architecture designs of the developed Polar, LDPC, and Turbo codes (and their variants).

### WP3: Link-Level Simulations and Performance Comparisons

The key objective is to validate and accurately assess the codes and algorithms developed in WP2. WP3 develops and implements a detailed simulation environment in order to assess the communications performance, particularly focusing on BER and/or FER for the different codes and encoding/decoding algorithms developed in WP2.

### WP4: Prototyping/Virtual Hardware Design

WP4 provides such implementation parameters related to CMOS technology node to WP2 in order to provide WP2 with a better view of the implementation limits and feasibility.

### WP5: Communication, Dissemination & Exploitation

The communication, dissemination, and exploitation tasks of EPIC are part of this WP with the objectives of ensuring utmost academic and commercial benefits both from EPIC and European perspective. WP5 puts special emphasis on a detailed exploitation plan for EPIC both in academic and industry channels.

### WP6: Project, Risk, and IPR Management

WP6 will be dedicated to the project management and relations to H2020 board, it will be managed by Technikon and will cover the global period of the project from M01 to M36.

## Contact:

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## Project Partners:



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InterDigital Europe Ltd.,  
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 Belgium [Leuven]



Polaran Ltd.,  
 Turkey [Ankara]



Technische Universität  
 Kaiserslautern,  
 Germany [Kaiserslautern]



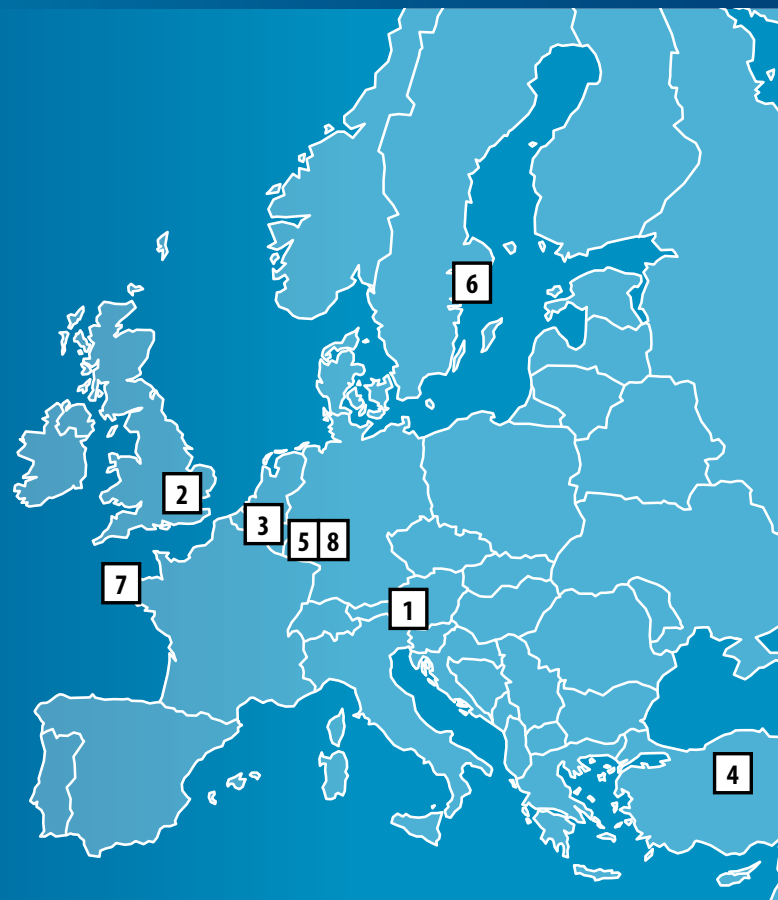
Ericsson AB,  
 Sweden [Stockholm]



Institut Mines-Télécom,  
 IMT Atlantique,  
 [Brest]



Creonic GMBH,  
 Germany [Kaiserslautern]



## Consortium:

The consortium of the EPIC project brings together a European team of recognized organizations and respected universities with scientific and technological backgrounds, making it well-positioned to achieve its objectives. All in all there are eight partners from seven different countries (Austria, Belgium, France, Germany, Sweden, Turkey and the United Kingdom) including three SMEs, two industrial partners, one research institution and two universities.